AN DIGITAL FREQUENCY SYNTHESIZING CIRCUIT AND SYSTEM THEREOF USING INTERPOLATION AND LINEAR FEEDBACK SHIFT REGISTER (LFSR)

CROSS-REFERENCE TO RELATED APPLICATION

This application claims the priority benefit of Taiwan application serial no. 92122055, filed August 12, 2003.

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The present invention relates to an all-digital frequency synthesizer. More particularly, the present invention relates to an digital frequency synthesizer that consists only simple logics and a linear feedback shift register, which provides lower complexity and superior resolution of frequency.

Description of Related Art

[0002] Traditionally, either a direct frequency synthesizer, a phase-locked frequency synthesizer, or a digital synthesizer is used to synthesize frequencies. An example of a conventional direct frequency synthesizer is shown in the block diagram in **FIG. 2**. Providing a frequency 26.7457 kHz is to be synthesized herein, a direct frequency synthesizer utilizes successive approximation to get finer frequency, and thus desired frequency is approached. However, the hardware of this method is obviously complex.

[0003] For another example of prior frequency synthesizer, phase-locked technique is applied therein. Referring to **FIG. 3**, a bock diagram of a phase-locked frequency syn-

thesizer is illustrated. This synthesizer incorporates a frequency divider with a Phase-Locked-Loop (PLL) circuit. The reference frequency, the synthesized frequency, and the minimal resolution in this case are f_1, f_2, and Δf respectively. This architecture is usually implemented with analog circuitry and is also relatively disorderly as opposed to what is proposed in this present invention.

[0004] A digital synthesizer further realizes frequency synthesis function besides direct frequency synthesizer and phase-locked frequency synthesizer. The block diagram of a generic digital synthesizer is shown in **FIG. 4**. Notice that this architecture is similar to a Numerically Controlled Oscillator (NCO). The reference frequency f_1 and the incremental frequency $\Delta\theta$ are predetermined in this system. The synthesized frequency f_2 is thus generated via continuously looking up in a cosine-table. However, when a finer resolution is to be synthesized, say 201.3457kHz, the cosine-table becomes large and this makes the hardware infeasible.

[0005] Concluding the three prior frequency synthesizers, complex scheme, analog circuitry, and low capability of target frequency are observed, which are undesirable unfortunately. Thus an all-digital frequency synthesizer complying feasible digital circuitry and finer resolution is proposed in this present invention.

SUMMARY OF THE INVENTION

[0006] As embodied and broadly described herein, the invention provides an all-digital circuit of frequency synthesizer using interpolation technique and Linear Feedback Shift Register (LFSR). The basic concept of this synthesizer is to store two sequences in a bank of memory or shift register. Using the idea of interpolation, all synthesizable fre-

quencies located between two predetermined threshold frequencies can be obtained, and resolution is determined by the order of LFSR thereby. A all-digital frequency synthesizing system is also included.

[0007] The basic architecture of frequency synthesizer in this present invention is shown in **FIG. 1**. The block **130** 'Seq.+' and block **132** 'Seq.–' are memory devices that store samples of the two reference frequencies $sin(2\pi\hat{f}_1 t)$ and $sin(2\pi\hat{f}_1 t)$. Theoretically all the frequencies lie between $\hat{f}_1$ and $\hat{f}_2$ can be synthesized using this architecture. The minimal resolution in frequency is $\frac{|\hat{f}_1 - \hat{f}_2|}{2^N}$, where N is the order of the LFSR **140**. The output of multiplexor (MUX) **110** is determined by the value in the LFSR **140**. When the value in the LFSR **140** is less than a threshold value, the data in 'Seq.–' **130** is passed; otherwise, the data in 'Seq.+' **132** passed, clocked by the rate 'Digi_clk'. When one sequence is completed, the value in LFSR **140** is shifted by one position and then is compared with the predetermined threshold again. With the method described herein, an all-digital, less complexity and superior resolution frequency synthesizer is embodied.

[0008] These and other objects, features and advantages of the present invention will become apparent from the following detailed description of illustrative embodiments thereof, which is to be read in connection with the accompanying drawings.

[0009] It is to be understood that both the foregoing general description and the following detailed description are exemplary, and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention.

[0011] **FIG. 1** is a block diagram **100** illustrating a frequency synthesizer according to one preferred embodiment in this present invention.

[0012] **FIG. 2** is a block diagram **200** illustrating a direct frequency synthesizer for one prior art example.

[0013] **FIG. 3** is a block diagram **300** illustrating a frequency synthesizer using PLL for another prior art example.

[0014] **FIG. 4** is a block diagram **400** illustrating a generic digital frequency synthesizer for yet another prior art example.

[0015] **FIG. 5** is a block diagram **500** illustrating a LFSR using Galois configuration according to one preferred embodiment in this present invention.

[0016] **FIG. 6A** is a diagram showing Discrete Fourier Transform (DFT) of the output signal of the frequency synthesizer in time domain according to one preferred embodiment in this present invention.

[0017] **FIG. 6B** is a diagram showing Discrete Fourier Transform (DFT) of the output signal of the frequency synthesizer in frequency domain according to one preferred embodiment in this present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0018] The present invention provides a simpler frequency synthesizer capable of synthesizing a high-precision signal as shown in **FIG. 1**. Assuming an output sequence with bitwidth 2 is to be generated, and the system clock is 13.392MHz, the reference frequencies are thus 13392/66=202.909 kHz and 13392/67=199.881 kHz. Also assuming the target output signal is designated 201 kHz herein. Thus the values in 'Seq.–' **130** and 'Seq.+' **132** in **FIG. 1** are represented as "00000000000000001111111111111111000000000000000-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1" and "000000000000000001111111111111111000000000000000-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1" respectively. For notation simplicity, these two sequences are also represented as "16/17/16/17" and "17/17/16/17" respectively. Since 11392/201=66.6269, the probability to generate output "Seq.–" is 0.6269. Similarly, the probability to generate "Seq.+" is 0.3731 (i.e. 1–0.6269). If we assign the order of the LFSR **140** to be 10 and the generating polynomial to be $g(D)=1+D^3+D^{10}$, the LFSR **140** may be plotted as the diagram in **FIG. 5** accordingly. Notice that a Galois configuration is presented this LFSR **140**, while a Fibonacci configuration is also feasible for a LFSR. Since the order of the LFSR is set to 10, the minimal frequency resolution is thus $(202.909-199.881)/2^{10}=0.002957\,\text{kHz}$. The threshold in this design is thus set to $round(0.3731*1024)/1024=0.3730_{(10)}=0101111110_{(2)}$.

[0019] In order to examine the accuracy of the synthesized frequency, a Discrete Fourier Transform (DFT) of the output signal is provided in **FIG. 6**. Notice that if performing zoom-in around 201kHz on the x-axis and compare the synthesized spectrum with that of $\sin(2\pi\cdot 201k\cdot t)$, an exact match is observed.

[0020] It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention covers modifications and variations of this invention provided they fall within the scope of the following claims and their equivalents.